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EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,895	JACOBSON ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 and 7-13 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment A as received on 11/24/2003 and Request for Extension of Time as received on 11/24/2003.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

5. The amendment filed 11/24/2003 is objected to under 35 U.S.C. § 132 because it introduces new matter into the disclosure. 35 U.S.C. § 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "in a byte stream" on line 4 of p.19 of the specification. The applicant asserts on p.11 of the current amendment that support for the amendments to the specification can be found in Figs.3-6b. However, Fig.6b does not provide any indication that the figure refers to a byte stream. Furthermore, the specification on p.18-19

simply says that the data structure in Fig.6b is another implementation of the linked list of Fig.6a, of which the specification does not refer to in any way as a byte stream. Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 7-10 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The limitation, "computer readable medium containing a backing register file instruction" is non-statutory subject matter. Here, the "backing register file instruction" is nonfunctional descriptive material which does not impart any functionality on the computer, nor does it define any physical or logical relationship with the computer or computer-readable medium (see MPEP § 2106). The claim itself does not describe the execution of the "backing register file instruction" resulting in a configuration change of the computer. That is, there is no use or intended use of the instruction as claimed which results in a change of the computer's configuration. Furthermore, the instruction as claimed does not have any real world application because the specification does not explicitly limit the category of "backing register file instructions" to be a specific set of instructions directed towards moving data between a memory of some type and a backing register file. The examiner suggests amending the claim language to, "A computer readable medium containing an executable backing register file instruction for moving data between a memory and a backing register file," or something of a similar nature.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "byte stream" is new matter and was not disclosed in the original specification, having only been added improperly as a result of the current amendment (see above objection to the specification, paragraph 5).

10. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claim contains the limitation "wherein the singly linked list and the byte stream contain backing register instructions." However, p.19 of the specification describes the invention having singly-linked list containing a set of fields of specified length containing addresses of registers to read from or write to between the Backing Register file and the Register file. These sets of fields are addresses, which are clearly not instructions as claimed, and therefore the claim language is not enabled within the specification and requires correction.

11. Furthermore, claim 10 contains the limitation "comprising a set of instructions for a singly linked list **and** a byte stream." However, p.19 of the specification describes the singly linked list and the data structure of Fig.6b (which in the amended specification is referred to as "a byte stream", see above paragraph 5 for new matter objection) as alternate embodiments of the same list of addresses, and does not describe both the linked list and the data structure of Fig.6b as being enabled at the same time. Therefore, the claim language is not enabled within the specification and requires correction. For the purposes of this examination, the Examiner will assume that the "and" in the claim language is really the alternative claim language, "or", so as to align with the teaching in the specification.

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites the limitation, "comprising a set of instructions for a singly linked list and a byte stream." It is unclear from the claim language whether the set of instructions are for use within a linked list and byte stream, whether they create or modify the linked list and byte stream, or something else completely. Please correct the claim language to more distinctly point out what the Applicant regards as the invention.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1-2, 5, 7-8 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Sollars, U.S. Patent No. 5,900,025.

16. Regarding claim 1, Sollars has taught a processor comprising:

a. At least one register file (20a,b of Fig.1),

b. At least one execution unit (14 of Fig.1),

c. At least one bypass circuit operatively coupled to said at least one register file and said at least one execution unit, said at least one bypass circuit capable of arbitrating access to said at least one register file (see Col.3 lines 35-58 and Col.5 lines 32-54). Here, because arbitration of access to the register files amongst threads is occurring, there is inherently some circuitry associated with the arbitration process in order for it to be carried out.

d. A backing register file (22a of Fig.1) operatively coupled to said at least one register file (see Fig.1), and where said backing register file is operationally and responsively coupled to at least one user-visible instruction (see Col.3 lines 25-34, Col.5 lines 21-31 and Col.14 lines 59-63).

17. Regarding claim 2, Sollars has taught the processor as in claim 1, further comprising:

a. A plurality of register files (20a,b of Fig.1),

b. At least one execution unit operably connected to each register file of said plurality of register files (see Fig.1), and where said backing register file is operably connected to each register file of said plurality of register files (see

Fig.1) providing thereby the ability to transfer values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any designated register file of said plurality of register files (see Col.3 lines 25-34).

18. Regarding claim 5, Sollars has taught a method for moving values from designated locations in designated register files (22a,b of Fig.1) to designated locations in a backing register file (20a of Fig.1) and values in designated locations in said backing register file to designated locations in designated register files (see Col.3 lines 25-34) comprising:

a. Identifying a backing register file instruction in a sequence of instructions. While not stated explicitly, it is inherent in the decoding operation (see Col.6 lines 16-18) that the instruction be identified, for without the identification of an instruction a computer would only be able to execute at most one type of instruction, effectively making it useless. Furthermore, it is inherent that the "MOV" instruction performs the same function as a backing register file instruction (see Col.14 lines 59-67), and that the instruction contains both source and destination fields allowing the user to identify the specific register from and to which the transfer will take place (see Figs.16b and 16c).

b. Decoding said backing register file instruction (see Col.6 lines 16-18), where if said backing file instruction is one of load-backing-register-file or load-register-file, making available addresses for specified numbers of locations in specified register files and an equal number of addresses for specified locations in said

backing register file, where said number of addresses is at least one. Because the instructions describe the transfer of data from one register to another (see Col.3 lines 25-34), it is inherent that not only must the instructions have at least one address for both the source and destination of the operation necessary for the instruction to execute encoded within the instruction, but that there is a minimal amount of decoding that is necessary in order to extract these addresses.

c. Reading values from each of said addresses ins said specified register file and writing said values to said equal number of addresses in said backing register file as specified by said backing register file instruction, if said backing register file instruction is of type load-backing-register-file. As described above, these instructions describe the transfer of data from one register to another (see above paragraph 18b and Col.3 lines 25-34). Therefore, it is inherent that in the execute stage of an instruction's lifecycle during a move/load-type instruction that the data is moved from one specified address to another specified address using the addresses specified in the decoded instruction.

d. Reading values form each of said addresses specified in said backing register file and writing said values to said equal number of addresses in said specified register file, if said backing register file instruction is of type load-register-file. As described above, it is inherent that move/load-type instructions transfer data from one specified address to a second specified address using addresses specified in the decoded instruction (see above paragraphs 18b and 18c, and Col.3 lines 25-34).

19. Regarding claims 7-9, the previous Office Action did not apply any prior art rejections on the claims, as only claims 1-5 were statutory. Because the Applicant has now attempted to amend claims 7-9 in order to make them statutory, the Examiner will apply a prior art rejection. However, assuming that claims 7-9 are deemed statutory, the scope of the claim language is so broad that the limitations are encompassed in claims 1-5, which have already been shown to have been taught by the prior art of record, and thus the limitations have been met before. See paragraphs 30-31 below for the rejection of claim 9.

20. Regarding claim 7, Sollars has taught a computer-readable medium containing a backing register file instruction (see Col.5 lines 25-34 and Col.14 lines 37-67).

21. Regarding claim 8, Sollars has taught a computer-readable medium as in claim 7, further comprising the backing register file instruction for transferring register values between a register file and said backing register file (see Col.3 lines 25-34 and Col.14 lines 37-67).

22. Regarding claim 10, Sollars has taught a computer-readable medium of claim 7, further comprising a set of instructions for a singly linked list and a byte stream, wherein the singly linked list and the byte stream contain backing register instructions (see Col.6 lines 16-34). Here, the IFU fetches a plurality of instructions simultaneously, instructions which are a multiple bytes in size, and hence a byte stream. Furthermore, the instructions are "backing register instructions" which move data between the register files and the backing register file (Col.3 lines 25-34). Therefore, since the claim language is in the alternate form (see above paragraph 11), the limitations have been met by the prior art of record.

23. Regarding claim 11, Sollars has taught the processor of claim 1, further comprising the backing register file (22a of Fig.1) capable of being explicitly used by programs at all privilege

levels (see Col.3 lines 25-58). Here, programs at a user level (see Col.3 lines 25-28), as well as well as all threads, can access all parts of the control register file (see Col.3 lines 45-58).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 3-4, 9 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sollars, U.S. Patent No. 5,900,025 as applied to claims 1-2 above, and further in view of Wilhelm et al., U.S. Patent No. 5,956,747.

26. Regarding claim 3, Sollars has taught the processor as in claim 1, but has not explicitly taught wherein the processor further comprises:

a. A connection circuit having a first connection and a second connection, where said first connection is operably connected to said backing register file and said second connection is operably connected to a main memory.

27. However, Wilhelm has taught a register file (28 of Fig.2) and a register cache (52 of Fig.2) operably connected to a main memory (32 of Fig.2) so that the register values of the register file can be stored in any backing memory (see Col.5 lines 1-11). One of ordinary skill in the art would have recognized that in order to execute a non-trivial program, some sort of instruction memory is necessary to hold the programs instructions. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Sollars and operably

connect a main memory to the backing register file so that a non-trivial program can be stored and subsequently executed.

28. Regarding claim 4, Sollars has taught the processor as in claim 2, but has not explicitly taught wherein the processor further comprises:

a. A connection circuit having a first connection and a second connection, where said first connection is operably connected to said backing register file and said second connection is operably connected to a main memory.

29. However, Wilhelm has taught a register file (28 of Fig.2) and a register cache (52 of Fig.2) operably connected to a main memory (32 of Fig.2) so that the register values of the register file can be stored in any backing memory (see Col.5 lines 1-11). One of ordinary skill in the art would have recognized that in order to execute a non-trivial program, some sort of instruction memory is necessary to hold the programs instructions. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Sollars and operably connect a main memory to the backing register file so that a non-trivial program can be stored and subsequently executed.

30. Regarding claim 9, Sollars has taught a computer-readable medium as in claim 7, but has not explicitly taught wherein the computer-readable medium further comprises the backing register file instruction for transferring values between main memory and said backing register file.

31. However, Wilhelm has taught a register file (28 of Fig.2) and a register cache (52 of Fig.2) operably connected to a main memory (32 of Fig.2) so that the register values of the register file can be stored in any backing memory (see Col.5 lines 1-11). One of ordinary skill in

the art would have recognized that in order to execute a non-trivial program, some sort of instruction memory is necessary to hold the programs instructions. Furthermore, Official Notice is taken that it is well know in the art that instruction sets contain LOAD instructions in order to move program instructions from main memory into a register file. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Sollars and operably connect a main memory to the backing register file so that non-trivial program instructions can be stored in main memory, transferred to the backing register file using a LOAD instruction when needed and subsequently executed.

32. Regarding claim 12, Sollars has taught a method of accessing a backing register file (20a of Fig.1) comprising:

a. Identifying a backing register file instruction in an instruction stream. While not stated explicitly, it is inherent in the decoding operation (see Sollars Col.6 lines 16-18) that the instruction be identified, for without the identification of an instruction a computer would only be able to execute at most one type of instruction, effectively making it useless. Furthermore, it is inherent that the "MOV" instruction performs the same function as a backing register file instruction (see Sollars Col.14 lines 59-67), and that the instruction contains both source and destination fields allowing the user to identify the specific register from and to which the transfer will take place (see Sollars Figs.16b and 16c).

b. Switching modes to access a backing register file (see Sollars Col.3 lines 35-58). Here, Sollars teaches switching the context (or mode) in order for threads to access the backing register file.

33. Sollars has not explicitly taught the method comprising the step of moving values between a main memory and a backing register file. However, Wilhelm has taught a register file (28 of Fig.2) and a register cache (52 of Fig.2) operably connected to a main memory (32 of Fig.2) so that the register values of the register file can be transferred to and stored in any backing memory (see Col.5 lines 1-11). One of ordinary skill in the art would have recognized that in order to execute a non-trivial program, some sort of instruction memory is necessary to hold the programs instructions. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Sollars and operably connect a main memory to the backing register file so that a non-trivial program can be stored in the main memory, transferred to the backing register file when needed and subsequently executed.

34. Regarding claim 13, Sollars in view of Wilhelm has taught the method of claim 12, further wherein one mode emulates a legacy software (see Sollars Col.1 lines 12-25). Here, the mode is switched between threads in order to access the backing register file (see Sollars Col.3 lines 35-58), and the backing register file can be used in a backward compatible emulation mode (see Sollars Col.1 lines 21-23).

Response to Arguments

35. Applicant's arguments with respect to claims 1-4 filed on 11/24/2003 have been considered but are moot in view of the new ground(s) of rejection.

36. Applicant's arguments with respect to claim 5 filed on 11/24/2003 have been fully considered but they are not persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which

applicant relies (i.e., moving values regardless of type) are not recited in the rejected claim 5.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). See below.

37. Claimed subject matter, **not** the specification, is the measure of invention. Limitations in the specification **cannot** be read into the claims for the purpose of avoiding the prior art (*In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978)).

38. "It is the claims that measure the invention." *SRI Int'l v. Matshshita Elec. Corp.*, 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

39. "The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

40. "[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

41. "Limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be **confused with adding an extraneous limitation** appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

42. "It is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is **not** to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." *In re Paulsen*, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

Conclusion

43. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
2/27/04

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